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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,604	08/25/2003	Peter J. Hopper	NSC1-M3000 (P05657)	2816

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,604	HOPPER ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE f this communication appears on the cover she t with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/26/04 (filing)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the application on 8/26/2003.

Specification

The wording "The amount of current flowing between the source 110 and the drain 112 is proportional to the amount of resistance of the channel region 116" is unsupported by the Specification and counter to general conditions known in the art. Said wording should be corrected, however, without introducing new matter.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 1-8*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al (US 2001/0001196 A1) in view of Ichikawa (6,611,027 B2).

On claims 1, 5 and 7: Choi et al teach a MOSFET transistor (N.B. : gate insulation layer 102 is thermal oxide; see section [0035]) comprising (cf. Figure 6, cell array region "a"; and Figure 7): an active region 103 of the substrate 100 (section [0030]); perimeter isolation dielectric material 101 formed in the substrate along a perimeter of the active region to define a sidewall interface between the isolation

dielectric material 101 and the active region 103 (section [0030]); spaced-apart source and drain regions 150 (section [0032]) to define a substrate channel region therebetween, both the source region and drain region also being spaced apart from the sidewall interface (cf. Figure 6); and a conductive gate electrode 140 including a first portion that extends over the substrate channel region (short portion of any of the gate array members) and a second portion that extends continuously over the entire said sidewall interface between the isolation dielectric material and the active region (long portion) (cf. Fig. 7), the conductive gate electrode being separated from the substrate channel region by intervening gate dielectric material 152 (cf. section [0030]).
Choi et al do not specifically teach (a) said substrate to have a conductivity type opposite to that of said source and drain regions, nor that said perimeter isolation dielectric material be formed along the entire perimeter of the active region.

However, it would have been obvious to include limitations (a) and (b) in view of Ichikawa, who, in a patent on how to protect MOS transistors from electrostatic charges (see abstract), - hence pertinent to Choi et al, (a) that source/drain regions 21 and substrate 20 to have opposite conductivity type (see col. 7, l. 5-30 and col. 5, l. 20-25, with n-type being the first conductivity type; thus meeting the further limitation of claim 5 as well, while, with regard to claim 5 it is noted that it is well-known in the art that an overall interchange between n-type and p-type conductivities in a device in general does not carry patentable weight unless Applicant explain why said interchange is critical to the invention) and (b) that the perimeter isolation dielectric material 25 (col. 7, l. 19-21) formed in the substrate is extended along the entire perimeter of the active

region (loc.cit.) as part of an embodiment that increases electrostatic discharge protection (col. 8, l. 21-32).

Motivation to include limitation (a) is merely the enablement of a functioning MOSFET, and motivation to include limitation (b) derives from the obvious enhancement of protection when what needs to be protected is completely surrounded by the protecting material.

With regard to claim 7, said claim merely recites steps in the process of manufacturing the device as claimed. The device of claim 1 would necessarily have to be formed in order to function. Claim 7 fails to further limit the device of claim 7 other than simply form each of their components.

On claim 2: although the perimeter isolation material in Choi et al is implemented using shallow trench isolation (STI) technology while the use of thermal (i.p.: silicon) oxide is common in said STI technology they do not specifically teach that the perimeter isolation dielectric material comprises silicon dioxide. However, it would have been obvious to include the further limitation of this claim in view of Ichikawa et al, who do teach the use of field oxide (which is necessarily silicon dioxide in view of the silicide formed underneath metal from which it can be inferred that the most standard selection of silicon is made for the semiconductor material (cf. col. 7, l. 19-21 and 30-36).

On claim 3: the conductive gate electrode by Choi et al comprises polysilicon (cf. Figure 8 and section [0035]).

On claim 4: the gate dielectric material by Choi et al comprises silicon dioxide (see section [0035]).

On claims 6 and 8: Applicant's disclosure does not teach why the range as claimed is critical to the invention. Instead, Applicants merely state their belief that the range should be what is claimed (see page 8 of the Specification). In view of the absence of a teaching why a range is critical to the invention Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. Finally, with regard to claim 8, said claim merely recites steps in the process of manufacturing the device as claimed. The device of claim 6 would necessarily have to be formed in order to function. Claim 8 fails to further limit the device of claim 6 other than simply form each of their components.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Ichikawa (US 2003/0006463 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
January 9, 2005

Patent Examiner:

Johannes Mondt (Art Unit: 2826)